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DOCKET NO. 00-BN-055 (STMI01-00055) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	Anthony X. Jarvis
Serial No.	:	09/751,377
Filed	:	December 29, 2000
For	:	BYPASS CIRCUITRY FOR USE IN A PIPELINED PROCESSOR
Group No.	:	2183
Examiner	:	Aimee J. Li

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
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Alexandria, VA 22313-1450

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Effective on 12/08/2004.
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FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/751,377
Filing Date	December 29, 2000
First Named Inventor	Anthony X. Jarvis
Examiner Name	Aimee J. Li
Art Unit	2183
Attorney Docket No.	00-BN-055 (STMI01-00055)

METHOD OF PAYMENT (check all that apply)

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☑ Deposit Account Deposit Account Number: 50-0208 Deposit Account Name: Davis Munck P.C.

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____	/ 50 = _____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Appeal Brief fee	$500.00

SUBMITTED BY

Signature	William C. Munck	Registration No. (Attorney/Agent) 39,308	Telephone 972-628-3600
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MAIL STOP APPEAL BRIEF - PATENTS
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APPEAL BRIEF

The Appellant has appealed to the Board of Patent Appeals and Interferences from the decision of the Examiner dated June 30, 2005, finally rejecting Claims 1-4, 6-14, and 16-22. The Appellant filed a Notice of Appeal on October 31, 2005, which was received by the U.S. Patent and Trademark Office on November 3, 2005. The Appellant respectfully submits this brief on appeal with the appropriate statutory fee.

REAL PARTY IN INTEREST

This application is currently owned by STMicroelectronics, Inc. as indicated by an assignment recorded on May 7, 2001 in the Assignment Records of the U.S. Patent and Trademark Office at Reel 011769, Frame 0344.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1-4, 6-14, and 16-22 have been rejected pursuant to a final Office Action dated June 30, 2005. Claims 5 and 15 have been cancelled. Claims 1-4, 6-14, and 16-22 are presented for appeal. A copy of all claims is provided in Appendix A.

STATUS OF AMENDMENTS

No amendments were submitted and refused entry after issuance of the final Office Action dated June 30, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

Regarding Claim 1, a data processor 100 includes an instruction execution pipeline 400. (*Application, Page 24, Lines 20-22*). The instruction execution pipeline 400 includes a read stage 404, a write stage 407, and a first execution stage 405. (*Application, Page 24, Line 22 – Page 25, Line 4*). The first execution stage 405 includes E execution units capable of producing data results from data operands. (*Application, Page 11, Lines 9-11; Page 29, Lines 4-7*). The data processor 100 also includes a register file 505 that includes a plurality of data registers. (*Application, Page 11, Lines 11-12; Page 29, Lines 8-9*). Each data register is capable of being read by the read stage 404 via at least one of R read ports R0-R7 of the register file 505, and each data register is capable of being written by the write stage 407 via at least one of W write ports W0-W3 of the register file 505. (*Application, Page 11, Lines 12-17; Page 29, Lines 8-9*). In addition, the data processor 100 includes bypass circuitry 500. (*Application, Page 27, Line 22 – Page 28, Line 6*). The bypass circuitry 500 is capable of receiving data results from output channels of source devices in at least one of the write stage 407 and the first execution stage 405. (*Application, Page 28, Lines 6-9; Page 28, Line 21 – Page 29, Line 1*). The bypass circuitry 500 includes a first plurality of bypass tristate line drivers 511B-511I. (*Application, Page 28, Lines 6-8*). The bypass tristate line drivers 511B-511I have input channels coupled to first output channels of a first plurality of the source devices, and the bypass tristate line drivers 511B-511I have tristate output channels coupled to a first common read data channel in the read stage 404. (*Application, Page 11, Line 19 – Page 12, Line 2; Page 28, Lines 6-18*). The bypass circuitry 500 also includes a first multiplexer 531 having a first input channel coupled to the first common read data channel and an output channel coupled to a first operand

channel of a first execution unit in the first execution stage 405. (*Application, Page 12, Line 19 – Page 13, Line 1; Page 28, Line 19 – Page 29, Line 7*).

Regarding Claim 11, a processing system 10 includes a data processor 100, a memory 130 coupled to the data processor 100, and a plurality of memory-mapped peripheral circuits 111-114 coupled to the data processor 100 for performing selected functions in association with the data processor 100. (*Application, Page 17, Line 9 – Page 18, Line 4*). The data processor 100 includes an instruction execution pipeline 400. (*Application, Page 24, Lines 20-22*). The instruction execution pipeline 400 includes a read stage 404, a write stage 407, and a first execution stage 405. (*Application, Page 24, Line 22 – Page 25, Line 4*). The first execution stage 405 includes E execution units capable of producing data results from data operands. (*Application, Page 11, Lines 9-11; Page 29, Lines 4-7*). The data processor 100 also includes a register file 505 that includes a plurality of data registers. (*Application, Page 11, Lines 11-12; Page 29, Lines 8-9*). Each data register is capable of being read by the read stage 404 via at least one of R read ports R0-R7 of the register file 505, and each data register is capable of being written by the write stage 407 via at least one of W write ports W0-W3 of the register file 505. (*Application, Page 11, Lines 12-17; Page 29, Lines 8-9*). In addition, the data processor 100 includes bypass circuitry 500. (*Application, Page 27, Line 22 – Page 28, Line 6*). The bypass circuitry 500 is capable of receiving data results from output channels of source devices in at least one of the write stage 407 and the first execution stage 405. (*Application, Page 28, Lines 6-9; Page 28, Line 21 – Page 29, Line 1*). The bypass circuitry 500 includes a first plurality of bypass tristate line drivers 511B-511I. (*Application, Page 28, Lines 6-8*). The bypass tristate line drivers 511B-511I have input channels coupled to first output channels of a

first plurality of the source devices, and the bypass tristate line drivers 511B-511I have tristate output channels coupled to a first common read data channel in the read stage 404. (*Application, Page 11, Line 19 – Page 12, Line 2; Page 28, Lines 6-18*). The bypass circuitry 500 also includes a first multiplexer 531 having a first input channel coupled to the first common read data channel and an output channel coupled to a first operand channel of a first execution unit in the first execution stage 405. (*Application, Page 12, Line 19 – Page 13, Line 1; Page 28, Line 19 – Page 29, Line 7*).

GROUNDS OF REJECTION

1. Claims 1-4, 6-10, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,805,852 to Nakanishi ("*Nakanishi*") in view of U.S. Patent No. 6,167,501 to Barry et al. ("*Barry*").

2. Claims 11-14, 16-20, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakanishi* and *Barry* in further view of U.S. Patent No. 4,591,973 to Ferris, III et al. ("*Ferris*").

ARGUMENT

I. GROUND OF REJECTION #1

The rejection of Claims 1-4, 6-10, and 21 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

A. OVERVIEW

Claims 1-4, 6-10, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,805,852 to Nakanishi ("*Nakanishi*") in view of U.S. Patent No. 6,167,501 to Barry et al. ("*Barry*").

B. STANDARD

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Appellant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the Appellant is entitled to grant

of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. (*MPEP § 2142*).

C. THE *NAKANISHI* REFERENCE

Nakanishi recites a bypass control circuit for a processor. (*Abstract*). The bypass control circuit is capable of providing data from result buffers e1-e4 and m1-m4 in an execution stage EX and a memory access stage MEM of the processor to latch circuits L1-L8. (*Abstract; Figure 3*). The latch circuits L1-L8 then provide the data to arithmetic and logic units (ALUs) a1-a4 of the processor. (*Figure 3*). Multiple buses 1-1 through 4-2 are used to provide the data to the latch circuits L1-L8. (*Figure 3*). Each of the buses 1-1 through 4-2 is associated with a particular one of the latch circuits L1-L8. (*Figure 3; Col. 10, Lines 21-60*). In addition, tristate buffers T1-T72

connect various sources of data to each of the buses 1-1 through 4-2. (*Figure 3; Col. 10, Lines 21-60*).

D. THE *BARRY* REFERENCE

Barry recites a "processing element" to "processing element" switch connection control mechanism. (*Abstract*). Among other things, the mechanism of *Barry* uses a multiplexer 20, which is used to control the data passed along a data input 14 to a processing element 4. (*Col. 7, Lines 33-52*).

E. CLAIMS 1-4, 6-10, AND 21

Claim 1 recites a data processor, which includes:

> an instruction execution pipeline comprising:
> a read stage;
> a write stage; and
> a first execution stage comprising E execution units capable of producing data results from data operands;
> a register file comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline via at least one of R read ports of said register file and each of said data registers capable of being written by said write stage of said instruction pipeline via at least one of W write ports of said register file; and
> bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising:
> a first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of said source devices and tristate output channels coupled to a first common read data channel in said read stage; and

> a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage.

The Examiner asserts that *Nakanishi* discloses "bypass circuitry" that includes a "plurality of bypass tristate line drivers" as recited in Claim 1. (*06/30/05 Office Action, Page 3, Section 5c*). The Examiner acknowledges that *Nakanishi* does not disclose a "multiplexer" as recited in Claim 1. (*06/30/05 Office Action, Page 3, Section 6*). The Examiner asserts that *Barry* discloses the use of a multiplexer and that it would be obvious to modify *Nakanishi* with *Barry* to render Claim 1 obvious. (*06/30/05 Office Action, Page 3, Section 6*). In particular, the Examiner asserts that it would be obvious to modify *Nakanishi* to incorporate the multiplexer of *Barry* because the modification would "lower implementation costs." (*06/30/05 Office Action, Pages 3-4, Section 6*). The Examiner also asserts that it would be obvious to modify *Nakanishi* to incorporate the multiplexer of *Barry* because "a multiplexer would be preferable to tri-state controls for buses." (*06/30/05 Office Action, Pages 13-14, Section 25*).

Nakanishi uses tristate buffers T1-T72 to provide data from different sources to the buses 1-1 through 4-2. More specifically, the tristate buffers T1-T72 of *Nakanishi* are used to ensure that only one data source provides data to any one of the buses 1-1 through 4-2 at a given time. For example, tristate buffers T1, T9, T17, T25, T33, T41, T49, T57, and T65 ensure that only one data source is providing data to bus 1-1 at a given time.

Also, each of the buses 1-1 through 4-2 in *Nakanishi* provides data to one of the latch circuits L1-L8. In particular, each bus is capable of providing data only to a specific one of the latch circuits

L1-L8. For example, bus 1-1 provides data only to latch circuit L1, and bus 4-2 provides data only to latch circuit L8. The buses 1-1 and 4-2 do not provide data to any other destinations in the processor of *Nakanishi*.

Presumably, the Examiner relies on the tristate buffers T1-T72 of *Nakanishi* as anticipating the "plurality of bypass tristate line drivers" recited in Claim 1. The Examiner also presumably relies on any of the buses 1-1 through 4-2 of *Nakanishi* as anticipating the "common read data channel" recited in Claim 1. Based on this, the Examiner must show that it would be obvious to modify *Nakanishi* to include the multiplexer of *Barry* between the buses 1-1 through 4-2 and the latch circuits L1-L8 of *Nakanishi*. The Examiner must make this showing in order to establish that the proposed *Nakanishi-Barry* combination discloses, teaches, or suggests both (i) a "plurality of bypass tristate line drivers" having output channels coupled to a "common read data channel," and (ii) a "multiplexer" having an input channel coupled to the "common read data channel" as recited in Claim 1.

The Examiner cannot make this showing. The tristate buffers T1-T72 of *Nakanishi* function so that data from only one source is provided on each of the buses 1-1 through 4-2, and each bus provides data to a single destination. For example, tristate buffers T1, T9, T17, T25, T33, T41, T49, T57, and T65 ensure that only one data source provides data to bus 1-1, and bus 1-1 provides that data only to latch circuit L1. Similarly, tristate buffers T2, T10, T18, T26, T34, T42, T50, T58, and T66 ensure that only one data source provides data to bus 1-2, and bus 1-2 provides that data only to latch circuit L2.

There is absolutely no need to insert a multiplexer between any of the buses 1-1 through 4-2

and the latch circuits L1-L8 of *Nakanishi*. For example, any multiplexer placed between bus 1-1 and the latch circuit L1 would receive only one input signal (the signal from bus 1-1). There would be no need for a multiplexer coupled to latch L1 to receive the signals from the other buses 1-2 through 4-2 because those buses 1-2 through 4-2 never provide data to the latch circuit L1 in *Nakanishi*. The whole purpose of a multiplexer is to receive multiple inputs and select one of the inputs for output. If there is only one input signal, there is no need for a multiplexer. Since there is only one input signal that can possibly be provided to latch circuit L1 in *Nakanishi* (the signal received over bus 1-1), there is clearly no need for a multiplexer between the latch circuit L1 and bus 1-1.

In order to justify placing a multiplexer between the buses 1-1 through 4-2 and the latch circuits L1-L8 in *Nakanishi*, the Examiner would have to propose removing some of the tristate buffers T1-T72 of *Nakanishi* in a way that enables each latch circuit L1-L8 to receive data from multiple buses 1-1 through 4-2. Only then would there actually be a need for a multiplexer between the buses 1-1 through 4-2 and the latch circuits L1-L8 of *Nakanishi*. The Examiner would then have to propose including the multiplexer of *Barry* in the circuit of *Nakanishi* to compensate for the missing tristate buffers. In addition, the Examiner must show that it would be obvious to replace some (but not all) of the tristate buffers T1-T72 of *Nakanishi* with the multiplexer of *Barry* since Claim 1 recites both a "plurality of bypass tristate line drivers" and a "multiplexer."

The Examiner asserts that using the multiplexer of *Barry* in the circuit of *Nakanishi* would lower implementation costs and would be preferable to tri-state controls. At most, this suggests that all of the tristate buffers T1-T72 of *Nakanishi* should be replaced with the multiplexer of *Barry*. The Examiner has never provided an explanation as to why a person skilled in the art would replace some

(but not all) of the tristate buffers T1-T72 of *Nakanishi* with the multiplexer of *Barry* so that the resulting combination includes both a "plurality of bypass tristate line drivers" and a "multiplexer" as recited in Claim 1.

In response to the Appellant's prior arguments, the Examiner states "Barry shows that, under certain conditions, it would have been obvious to a person of ordinary skill in the art that the multiplexers [of *Barry*] would be a beneficial use instead of the tristates [of *Nakanishi*]." (*10/03/05 Advisory Action, Page 2, First paragraph*) (underlining added). Once again, this shows that a person skilled in the art might be motivated to replace all of the tristate buffers T1-T72 of *Nakanishi* with the multiplexer of *Barry*. It does not establish that a person skilled in the art would replace only some of the tristate buffers T1-T72 of *Nakanishi* with the multiplexer of *Barry* to form a circuit having both a "plurality of bypass tristate line drivers" and a "multiplexer" as recited in Claim 1.

The Examiner also argues "[t]o state that a person of ordinary skill in the art would just replace all tristate buffers [in *Nakanishi*] with multiplexers [of *Barry*] without a second thought to the conditions relayed in Barry and of Nakanishi is not taking into consideration the full teachings and just incorporating one reference into another." (*10/03/05 Advisory Action, Page 2, First paragraph*). The Examiner fails to identify any portion of *Nakanishi* or *Barry* explaining why a person skilled in the art would replace only some of the tristate buffers T1-T72 of *Nakanishi* with the multiplexer of *Barry*. More specifically, the Examiner fails to identify what the "conditions relayed" in *Barry* are that would provide this motivation. The Examiner also fails to identify the teachings of *Nakanishi* that would provide this motivation. Instead, the only motivations actually identified by the Examiner for using the multiplexer of *Barry* in the circuit of *Nakanishi* are lower implementation

costs and a preference for multiplexers over tri-state controls. Neither of these motivations suggests replacing only some of the tristate buffers T1-T72 of *Nakanishi* with the multiplexer of *Barry*.

Under 35 U.S.C. § 103, the burden is specifically placed on the Examiner to establish that each and every limitation of Claim 1 is disclosed, taught, or suggested in the cited references. The Examiner cannot satisfy this burden by simply citing one reference that discloses tristate buffers, citing another reference that discloses multiplexers, and making an assertion that a person skilled in the art would combine the references to produce a circuit having both tristate buffers and multiplexers.

The Examiner must specifically show that a person skilled in the art would modify *Nakanishi* with *Barry* to reach the invention claimed in Claim 1. The Examiner must also specifically show that there is a motivation to make this modification. The fact is that there is absolutely no need to modify *Nakanishi* so that the circuit of *Nakanishi* includes both the tristate buffers T1-T72 of *Nakanishi* and the multiplexers of *Barry*. Without this need, the Examiner cannot satisfy the burden of showing that a person skilled in the art would modify *Nakanishi* to include both a "plurality of bypass tristate line drivers" and a "multiplexer" as recited in Claim 1.

For these reasons, the Examiner fails to establish that the proposed *Nakanishi-Barry* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 1 (and its dependent claims). Accordingly, the Appellant respectfully requests that the final rejection of Claims 1-4, 6-10, and 21 be withdrawn and that Claims 1-4, 6-10, and 21 be passed to allowance.

II. GROUND OF REJECTION #2

The rejection of Claims 11-14, 16-20, and 22 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

A. OVERVIEW

Claims 11-14, 16-20, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Nakanishi* and *Barry* in further view of U.S. Patent No. 4,591,973 to Ferris, III et al. ("*Ferris*").

B. THE *FERRIS* REFERENCE

Ferris recites an input/output system for coupling a computer to a plurality of peripheral devices. (*Abstract*). The peripheral devices include digital-to-analog converters. (*Col. 1, Lines 11-13*).

C. CLAIMS 11-14, 16-20, AND 22

Claim 11 recites a processing system, which includes:

> a data processor, wherein said data processor comprises:
> an instruction execution pipeline comprising:
> a read stage;
> a write stage; and
> a first execution stage comprising E execution units capable of producing data results from data operands;
> a register file comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline via at least one of R read ports of said register file and each of said data registers capable of being written by

said write stage of said instruction pipeline via at least one of W write ports of said register file; and

bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising:

a first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of said source devices and tristate output channels coupled to a first common read data channel in said read stage; and

a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage;

a memory coupled to said data processor; and

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor.

As described above, the Examiner has not established that a person skilled in the art would modify *Nakanishi* with *Barry* to include both (i) a "plurality of bypass tristate line drivers" having output channels coupled to a "common read data channel," and (ii) a "multiplexer" having an input channel coupled to the "common read data channel" as recited in Claim 11.

The Examiner relies on *Ferris* only as allegedly disclosing the use of "peripheral circuits" as recited in Claim 11. (*06/30/05 Office Action, Page 8, Section 15*). The Examiner does not rely on *Ferris* as disclosing, teaching, or suggesting the use of both a "plurality of bypass tristate line drivers" having output channels coupled to a "common read data channel" and a "multiplexer" having an input channel coupled to the "common read data channel" as recited in Claim 11.

For these reasons, the Examiner has not establish that the proposed *Nakanishi-Barry-Ferris* combination discloses, teaches, or suggests the Appellant's invention as recited in Claim 11 (and its dependent claims). Accordingly, the Appellant respectfully requests that the final rejection of

Claims 11-14, 16-20, and 22 be withdrawn and that Claims 11-14, 16-20, and 22 be passed to allowance.

SUMMARY

The Appellant has demonstrated that the present invention as claimed is clearly distinguishable over the prior art cited of record. Therefore, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the final rejection of the Examiner and instruct the Examiner to issue a notice of allowance of all claims.

The Appellant has enclosed the appropriate fee to cover the cost of this APPEAL BRIEF. The Appellant does not believe that any additional fees are due. However, the Commissioner is hereby authorized to charge any additional fees (including any extension of time fees) or credit any overpayments to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: Dec. 30, 2005

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APPENDIX A

PENDING CLAIMS APPENDIX

1. A data processor comprising:
an instruction execution pipeline comprising:
a read stage;
a write stage; and
a first execution stage comprising E execution units capable of producing data results from data operands;
a register file comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline via at least one of R read ports of said register file and each of said data registers capable of being written by said write stage of said instruction pipeline via at least one of W write ports of said register file; and
bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising:
a first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of said source devices and tristate output channels coupled to a first common read data channel in said read stage; and
a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage.

2. The data processor as set forth in Claim 1 wherein said bypass circuitry further comprises a second plurality of bypass tristate line drivers having input channels coupled to said first output channels of said first plurality of said source devices and tristate output channels coupled to a second common read data channel in said read stage.

3. The data processor as set forth in Claim 2 further comprising a first register file tristate line driver having an input channel coupled to a first one of said R read ports and an output channel coupled to said first common read data channel in said read stage.

4. The data processor as set forth in Claim 3 further comprising a second register file tristate line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage.

5. (Cancelled).

6. The data processor as set forth in Claim 4 further comprising a second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage.

7. The data processor as set forth in Claim 6 wherein said bypass circuitry further comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer.

8. The data processor as set forth in Claim 7 wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer.

9. The data processor as set forth in Claim 8 wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer.

10. The data processor as set forth in Claim 9 wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer.

11. A processing system comprising:
a data processor, wherein said data processor comprises:
an instruction execution pipeline comprising:
a read stage;
a write stage; and
a first execution stage comprising E execution units capable of producing data results from data operands;
a register file comprising a plurality of data registers, each of said data registers capable of being read by said read stage of said instruction pipeline via at least one of R read ports of said register file and each of said data registers capable of being written by said write stage of said instruction pipeline via at least one of W write ports of said register file; and
bypass circuitry capable of receiving data results from output channels of source devices in at least one of said write stage and said first execution stage, said bypass circuitry comprising:
a first plurality of bypass tristate line drivers having input channels coupled to first output channels of a first plurality of said source devices and tristate output channels coupled to a first common read data channel in said read stage; and
a first multiplexer having a first input channel coupled to said first common read data channel and an output channel coupled to a first operand channel of a first execution unit in said first execution stage;
a memory coupled to said data processor; and
a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor.

12. The processing system as set forth in Claim 11 wherein said bypass circuitry further comprises a second plurality of bypass tristate line drivers having input channels coupled to said first output channels of said first plurality of said source devices and tristate output channels coupled to a second common read data channel in said read stage.

13. The processing system as set forth in Claim 12 further comprising a first register file tristate line driver having an input channel coupled to a first one of said R read ports and an output channel coupled to said first common read data channel in said read stage.

14. The processing system as set forth in Claim 13 further comprising a second register file tristate line driver having an input channel coupled to a second one of said R read ports and an output channel coupled to said second common read data channel in said read stage.

15. (Cancelled).

16. The processing system as set forth in Claim 14 further comprising a second multiplexer having a first input channel coupled to said second common read data channel and an output channel coupled to a second operand channel of said first execution unit in said first execution stage.

17. The processing system as set forth in Claim 16 wherein said bypass circuitry further comprises a first bypass channel coupling an output channel of said first execution unit to a second input channel of said first multiplexer.

18. The processing system as set forth in Claim 17 wherein said first bypass channel couples said output channel of said first execution unit to a second input channel of said second multiplexer.

19. The processing system as set forth in Claim 18 wherein said bypass circuitry further comprises a second bypass channel coupling an output channel of a second execution unit in said first execution stage to a third input channel of said first multiplexer.

20. The processing system as set forth in Claim 19 wherein said second bypass channel couples said output channel of said second execution unit to a third input channel of said second multiplexer.

21. The data processor of Claim 1, further comprising a latch coupled to the output channel of the first multiplexer and to the first operand channel of the first execution unit.

22. The processing system of Claim 11, further comprising a latch coupled to the output channel of the first multiplexer and to the first operand channel of the first execution unit.

APPENDIX B

EVIDENCE APPENDIX

None

APPENDIX C

RELATED PROCEEDINGS APPENDIX

None